LISTING OF THE CLAIMS

Please amend the claims as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) An insulated gate power transistor semiconductor device comprising a semiconductor body having an active area with a plurality of electrically parallel transistor cells, wherein each transistor cell has a source region and a drain region of a first conductivity type which are separated by a channel-accommodating body region adjacent an insulated gate structure, said gate structure comprising first and second gates isolated from each other so as to be independently operable, the first gate being an insulated trench-gate adjacent the body region enabling a first, vertical, channel portion to be formed in said body ~~portion~~ region when gate potential is applied to the first gate, the second gate having at least an insulated planar gate portion that is located above the first gate on a top major surface of the semiconductor body adjacent the body region, the second gate enabling a second, at least partly lateral, channel portion to be formed in said body portion when gate potential is applied to the second gate, such that simultaneous operation of the first and second gates combines the first and second channel portions to form a conduction channel between the source and drain regions.

2. (Previously presented) A semiconductor device as claimed in claim 1, wherein a said gate structure is located at the boundary between each two adjacent transistor cells, wherein at said boundary, an insulated trench having gate material therein forms said first gate for the two transistor cells, and a planar insulation layer with gate material thereon is located on top of the trench and extends laterally both ways beyond the trench, such that said second gate for the two transistor cells is an insulated substantially completely planar gate, and such that the planar insulation layer also isolates the first and second gates from each other for the two transistor cells.

3. (Currently amended) A semiconductor device as claimed in claim 1, wherein a said gate structure is located at the boundary between ~~the~~ each two adjacent transistor cells, wherein at said boundary, an insulated trench having gate material in a lower portion of

the trench provides said first gate for the two transistor cells, a first insulation layer is located laterally within and across the trench with gate material thereon in an upper part of the trench, and a second insulation layer with gate material thereon extends laterally both ways from the trench on the top major surface of the semiconductor body, ~~such that~~ said second gate for the two transistor cells ~~has~~ having an insulated trench-gate portion formed from the gate material in the upper part of the trench and ~~an~~ the insulated planar gate portion of the second gate being formed from the gate material on the second insulator, and ~~such that~~ wherein the first insulation layer ~~laterally within and across the trench~~ isolates the first and second gates from each other for the two transistor cells.

4. (Previously presented) A semiconductor device as claimed in any one of claims 1 to 3, wherein the transistor cells in the active area have a closed cell geometry in which said peripheral gate structures surround each transistor cell in a two-dimensionally repetitive pattern.

5. (Currently amended) A circuit arrangement including a power transistor semiconductor device as claimed in claim 1, wherein the first gates and the second gates of the transistor cells are respectively connected to first and second gate electrodes of the device, and wherein said first and second gate electrodes are arranged for connection to respective independent applied control potentials ~~(Vcc, V_F; 573,673)~~.

6. (Currently amended) A circuit arrangement as claimed in claim 5, wherein a terminal ~~means (Vcc, VF)~~ for connecting to a supplied a fixed gate potential is connected to the first gate electrode, and wherein a gate driver circuit for applying a modulating gate potential is connected to the second gate electrode.

7. (Previously presented) A circuit arrangement as claimed in claim 6, wherein the power transistor semiconductor device is a high side power transistor connected in series with a low side power transistor for supplying a regulated voltage to an output via a switch node connection between the high side and low side transistors, and wherein said gate driver

circuit is included in a control circuit for alternately switching the high side and low side transistors on and off.

8. (Currently amended) A circuit arrangement as claimed in claim 6, wherein the power transistor semiconductor device is a switch for supplying current to a load ~~(L)~~ when the load ~~(L)~~ is connected to one of a source electrode and a drain electrode of the device.

9. (Previously presented) A circuit arrangement as claimed in claim 8, wherein the gate driver circuit is included in a control circuit which is integrated with the power transistor switch in said semiconductor body.

10. (Currently amended) A circuit arrangement as claimed in claim 9, wherein the control circuit includes protection circuitry ~~means~~ for the power transistor switch.

11. (New) A semiconductor device as claimed in claim 1, wherein the drain regions of the plurality of transistor cells are located on a side of the semiconductor body that is opposite from the top major surface of the semiconductor body.

12. (New) A semiconductor device as claimed in claim 1, wherein the drain regions of the plurality of transistor cells are formed by a common drain region.

13. (New) An insulated gate power transistor semiconductor device comprising a semiconductor body having an active area with electrically parallel first and second transistors, the first and second transistors each having a source region and a drain region of a first conductivity type, the drain regions of the transistors being formed by a common drain region and the source and drain regions of each of the transistors being separated from each other by a channel-accommodating body region that is adjacent an insulated gate structure, the gate structure including first and second gates that are isolated from each other and that are independently operable, the first gate being an insulated trench-gate that enables a first, vertical, channel portion to be formed in the body region when a gate potential is applied to the first gate, the second gate having at

least an insulated planar gate portion that enables a second, at least partly lateral, channel portion to be formed in the body region when a gate potential is applied to the second gate, wherein simultaneous operation of the first and second gates combines the first and second channel portions to form a conduction channel between the source and drain regions of at least the first transistor, and wherein the second gate is located on a top surface of the semiconductor body above the first gate.

14. (New) A semiconductor device as claimed in claim 13, wherein the gate structure is located at a boundary between the first and second transistors, and the first gate is formed from an insulated trench having gate material therein that extends to the top surface of the semiconductor body, and wherein the device includes a planar insulation layer with gate material thereon that each extends laterally beyond both sidewalls of the trench on the top surface of the semiconductor body, the second gate being formed from the gate material on the planar insulation layer.

15. (New) A semiconductor device as claimed in claim 1, wherein the gate structure is located at a boundary between the first and second transistors, and wherein the first gate is formed from gate material in a lower portion of an insulated trench, a first insulation layer is located laterally within and across the gate material in the lower portion of the insulated trench, the second gate includes an insulated trench-gate portion formed from gate material on the first insulation layer in an upper portion of the insulated trench, and the insulated planar gate portion of the second gate is located on the top surface of the semiconductor body above the insulated trench.

16. (New) A semiconductor device as claimed in claim 13, wherein the common drain region is located on a side of the semiconductor body that is opposite from the top surface of the semiconductor body.